

## ***DETAILED ACTION***

### ***Status of Application***

1. This office action is in response to the filing of the application papers on 19 September 2006, Claims 1-20 are pending in this application.

### ***Foreign Priority***

2. Acknowledgement is made that the certified copy of the foreign priority document has been received.

### ***Information Disclosure Statement***

3. Acknowledgement is made that the information disclosure statements filed on 11/23/2005 has been received and considered by the examiner. If the applicant is aware of any prior art or any other co-pending applications not already of record, he/she is reminded of his/her duty under 37 CFR 1.56 to disclose the same.

### ***Specification***

4. The disclosure is objected to because of the following informalities: The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. Appropriate correction is required. The following title is suggested: "Nitride-Based Semiconductor Light-Emitting Device and Illuminating Device."

***Allowable Subject Matter***

5. Claim 20 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this

Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Hasegawa et al. (U.S. Pub. Application 2005/0269584 A1).

Art Unit: 2811

8. Regarding claim 1, Hasegawa et al. discloses a semiconductor light-emitting device comprising:

- a substrate (item 81) made of group III-V nitride semiconductor (pg. 11, paragraph [0144], lines 3-6; Fig. 14)
- a first n-type semiconductor layer (item 87) containing indium and formed over a main surface of the substrate (item 81) (pg. 12, paragraph [0144], lines 15-17; Fig. 14)
- a light-emitting layer (item 88) formed over the first n-type semiconductor layer (item 87) (pg. 12, paragraph [0144], lines 15-17; Fig. 14) .

9. Regarding claim 2, Hasegawa et al. discloses a semiconductor light-emitting device as described in reference to claim 1, wherein the substrate (item 81) is made of gallium nitride (pg. 11, paragraph [0144], lines 3-6; Fig. 14).

10. Regarding claim 3, Ueda et al. discloses a semiconductor light-emitting device as described in reference to claim 1, wherein the substrate (item 81) is a substrate whose main surface is polished (pg. 12, paragraph [0149])

11. Regarding claim 4, Ueda et al. discloses a semiconductor light-emitting device as described in reference to claim 3, wherein the substrate (item 81) is a substrate whose main surface is etched (pg. 12, paragraph [0146], lines 1-6, Figs. 16E-16F).

12. Regarding claim 5, Ueda et al. discloses a semiconductor light-emitting device as described in reference to claim 3, wherein the substrate (item 81) is a substrate whose main surface is planarized (pg. 12, paragraph [0148], lines 5-12).

Art Unit: 2811

13. Regarding claim 6, Hasegawa et al. discloses a semiconductor light-emitting device as described in reference to claim 1, wherein the light-emitting layer (item 88) has a multiple quantum well structure formed by alternately stacking a quantum well layer and a barrier layer, and the quantum well layer has a thickness of 1 to 2.5 nm inclusive (pg. 12, paragraph [0151], lines 14-16, Fig.

14).

14. Regarding claim 7, Hasegawa et al. discloses a semiconductor light-emitting device as described in reference to claim 1, wherein the first n-type semiconductor layer (item 87) is made of a compound whose general formula is represented by  $\text{In}_a\text{Al}_b\text{Ga}_{1-a-b}\text{N}$  ( $0 < a < 1$ ,  $0 \leq b < 1$ ,  $a + b \leq 1$ ) (pg. 12, paragraph [0144], lines 15-17 and paragraph [0151], lines 9-15; Fig. 14).

15. Regarding claim 8, Hasegawa et al. discloses a semiconductor light-emitting device as described in reference to claim 7, wherein the aluminum content of the first n-type semiconductor layer (item 87) is 3% or lower (pg. 12, paragraph [0144], lines 15-17 and paragraph [0151], lines 9-15; Fig. 14).

16. Regarding claim 9, Hasegawa et al. discloses a semiconductor light-emitting device as described in reference to claim 1, wherein the first n-type semiconductor layer (item 87) has a thickness of 10 nm to 1  $\mu\text{m}$  inclusive (pg. 12, paragraph [0151], lines 9-10).

17. Regarding claim 10, Hasegawa et al. discloses a semiconductor light-emitting device as described in reference to claim 1, further comprising a second n-type semiconductor layer (item 85) formed between the substrate and the first

Art Unit: 2811

n-type semiconductor layer (item 87) (pg. 12, paragraph [0144], lines 13-14 and lines 29-31 and paragraph [0151], lines 1-4, Fig. 14).

18. Regarding claim 11, Hasegawa et al. discloses a semiconductor light-emitting device as described in reference to claim 10, wherein the second n-type semiconductor layer (item 85) is made of a compound whose general formula is represented by  $\text{In}_c\text{Al}_d\text{Ga}_{1-c-d}\text{N}$  ( $0 \leq c < 1$ ,  $0 \leq d < 1$ ,  $c+d < 1$ ) (pg. 12, paragraph [0144], lines 13-14 and paragraph [0151], lines 1-4, Fig. 14).

19. Regarding claim 12, Hasegawa et al. discloses a semiconductor light-emitting device as described in reference to claim 11, wherein the second n-type semiconductor layer (item 85) is an n-type contact layer (pg. 12, paragraph [0144], lines 13-14 and lines 29-31; Fig. 14).

20. Regarding claim 13, Hasegawa et al. discloses a semiconductor light-emitting device as described in reference to claim 8, further comprising a third n-type semiconductor layer (item 85) formed between the first n-type semiconductor layer and the light-emitting layer (item 88) (pg. 12, paragraph [0144], lines 13-14 and lines 29-31; Fig. 14).

21. Regarding claim 14, Hasegawa et al. discloses a semiconductor light-emitting device as described in reference to claim 13, wherein the third n-type semiconductor layer (item 85) is an n-type contact layer (pg. 12, paragraph [0144], lines 13-14 and lines 29-31; Fig. 14).

22. Regarding claim 15, Hasegawa et al. discloses a semiconductor light-emitting device as described in reference to claim 1, further comprising a fourth n-type semiconductor layer (item 86) formed between the first n-type

Art Unit: 2811

semiconductor layer and the light-emitting layer. (pg. 12, paragraph [0144], lines 14-17 and paragraph [0151], lines 5-8; Fig. 14).

23. Regarding claim 16, Hasegawa et al. discloses a semiconductor light-emitting device as described in reference to claim 15, wherein the fourth n-type semiconductor layer is made of a compound whose general formula is represented by  $\text{Al}_e\text{Ga}_{1-e}\text{N}$  ( $0 \leq e < 1$ ) (pg. 12, paragraph [0144], lines 14-17 and paragraph [0151], lines 5-8; Fig. 14).

24. Regarding claim 17, Hasegawa et al. discloses a semiconductor light-emitting device as described in reference to claim 16, wherein the fourth n-type semiconductor layer is a cladding layer (pg. 12, paragraph [0144], lines 14-17 and paragraph [0151], lines 5-8; Fig. 14).

25. Regarding claim 18, Hasegawa et al. discloses a semiconductor light-emitting device as described in reference to claim 17, wherein the cladding layer (item 86) has a thickness of 5 to 200 nm inclusive (pg. 12, paragraph [0151], lines 5-8; Fig. 14).

26. Regarding claim 19, Hasegawa et al. discloses a semiconductor light-emitting device as described in reference to claim 1, further comprising:

- an n-type contact layer (item 85) which is formed between the substrate (item 81) and the light-emitting layer (item 88) and a portion of which is exposed (pg. 12, paragraph [0144], lines 13-14 and lines 29-31; Fig. 14)
- an n-side electrode (item 99) formed on the exposed portion of the n-type contact layer (item 85) (pg. 12, paragraph [0144], lines 29-31; Fig. 14);

Art Unit: 2811

- an n-type cladding layer (item 86) formed between the first n-type semiconductor layer (item 87) and the light-emitting layer (item 88) (pg. 12, paragraph [0144], lines 14-17 and paragraph [0151], lines 5-8; Fig. 14)
- a p-type semiconductor layer (item 91) formed on the light-emitting layer (item 88) (pg. 12, paragraph [0144], lines 21-23; Fig. 14);
- a p-side electrode (item 98) formed over the p-type semiconductor layer (item 91), wherein the device is mounted with an element formation surface thereof facing a submount for mounting (pg. 12, paragraph [0144], lines 26-28 and Fig. 14).

27. Claims 1, 2, and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsuda et al. (U.S. Pub. Application 2004/0051105 A1).

28. Regarding claim 1, Tsuda et al. discloses a semiconductor light-emitting device comprising:

- a substrate (item 700a) made of group III-V nitride semiconductor (pg. 12, paragraph [0139], lines 1-2; Figs. 8-14)
- a first n-type semiconductor layer (item 703) containing indium and formed over a main surface of the substrate (item 700a) (pg. 7, paragraph [0097], lines 10-14; Figs. 8-14)
- a light-emitting layer (item 706) formed over the first n-type semiconductor layer (item 703) (pg. 7, paragraph [0096], lines 5-7 and paragraph [0098]; Figs. 8-14).

Art Unit: 2811

29. Regarding claim 2, Tsuda et al. discloses a semiconductor light-emitting device as described in reference to claim 1, wherein the substrate (item 81) is made of gallium nitride (pg. 12, paragraph [0139], lines 1-4; Figs. 8-14).

30. Regarding claim 6, Ueda et al. discloses a semiconductor light-emitting device as described in reference to claim 1, wherein the light-emitting layer (item 706) has a multiple quantum well structure formed by alternately stacking a quantum well layer and a barrier layer, and the quantum well layer has a thickness of 1 to 2.5 nm inclusive (pgs. 7-8, paragraph [0098]; pg. 13, paragraph [0161]; Figs. 8-14).

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to VERNON P. WEBB whose telephone number is (571)270-3332. The examiner can normally be reached on Monday through Friday, 7:30 am to 5 pm, Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on 571-272-1760. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2811

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lynne A. Gurley/  
Supervisory Patent Examiner, Art Unit 2811

/V. Parris Webb/  
Examiner, Art Unit 2811